REMARKS

Claims 1-13 and 16-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,218,729 to Zavrel, Jr. et al. The grounds for rejection remain the same as set forth in the previous Office Action.

Applicants traverse, and respectfully request the Examiner to reconsider in view of the amendment to the claims and the following remarks.

In reference to Fig. 1 of the present specification, printed wiring substrate 120 comprises a capacitor accommodation cavity 121 having a bottom portion 122 and a bottom surface restriction portion 121S for accommodating capacitor 130. The built-in capacitor 130 is fixedly attached to printing wiring substrate 121 by means of an insulating filling resin 123 filled into a gap therebetween, such that the capacitor 130 is distinct from the printed wiring substrate 121. Printed wiring substrate 120 has a planar surface, and capacitor terminals 131 project beyond the planar surface of the printed wiring substrate 120.

The Examiner considered Zavrel as disclosing a printed wiring substrate 822 having a planar surface and a built-in capacitor 804 having a plurality of capacitor terminals 810, 812 projecting beyond the surface of the printed substrate. However, this is incorrect. These reference numbers designate substrate terminals (interconnects), and are not part of capacitor 804 shown in Fig. 8 of Zavrel. (Col. 4, lines 44-46). Rather, in Zavrel, vias 850 and 854 provide an electrical path to plates 860 and 862 of capacitor 804 (col. 4, lines 46-49). Not even these vias, which also are not part of capacitor 804, project beyond the planar surface of the printed wiring substrate as required by the present claims. In the present invention, the capacitor is directly connected to the IC chip, such that noise which may enter between the IC chip and the capacitor

can be suppressed to a significantly low level (page 6, lines 4-6 of the specification). This is because in the present invention, the capacitor terminals project beyond the surface of the printed wiring substrate to directly contact the connection-to-capacitor terminals of the IC chip as required by the present claims. As recited in claims 1, 2 and 4, the capacitor comprises (i) a pair of electrodes or electrode groups (e.g., parallel plates having a dielectric sandwiched therebetween); and (ii) capacitor terminals projecting beyond the planar surface of the printed wiring substrate.

Also, contrary to the Examiner's suggestion, the capacitor plates 860 and 862 in Zavrel are embedded in the laminated substrate 822 and a capacitor accommodation cavity is not disclosed. Zavrel also does not disclose a cavity periphery region as required by claim 7 or a capacitor position restriction portion which abuts the capacitor so as to restrict the position of the capacitor in a depth direction of the capacitor accommodation cavity as required by present claim 8.

To more clearly distinguish the invention over the applied prior art, claims 1, 2 and 4 have been amended to recite that the built-in capacitor is distinct from the printed wiring substrate; that the printed wiring substrate comprises a capacitor accommodation cavity for accommodating the capacitor; and that the plurality of capacitor terminals are bonded directly to a plurality of connection-to-capacitor terminals of the IC chip. Also, the claims have been further amended to more clearly recite that the capacitor itself comprises a plurality of capacitor terminals projecting beyond the surface of the printed wiring substrate.

Entry of the amendments at this stage of prosecution is respectfully requested as placing the case in condition for allowance.

Withdrawal of all rejections and allowance of claims 1-13 and 16-18 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Twice Amended) A printed wiring substrate having a planar surface and a built-in capacitor distinct from the printed wiring substrate on which an IC chip is mounted, said printed wiring substrate comprising a capacitor accommodation cavity for accommodating the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals projecting beyond the planar surface of the printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively flip-chip-bonded directly to a plurality of connection-to-capacitor terminals of the IC chip; and

the plurality of substrate terminals of the printed wiring substrate are respectively flip-chip-bonded to a plurality of connection-to-substrate terminals of the IC chip.

2. (Twice Amended) A printed wiring substrate having a planar surface and a built-in capacitor distinct from the printed wiring substrate on which an IC-chip-carrying printed wiring substrate is mounted, said printed wiring substrate comprising a capacitor accommodation cavity for accommodating the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals projecting beyond the planar surface of the printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip-carrying printed wiring circuit comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively bonded in a connection-face-to-connection-face manner directly to a plurality of connection-to-capacitor terminals of the IC-chip-carrying printed wiring substrate; and

the plurality of substrate terminals of the printed wiring substrate are respectively bonded in a connection-face-to-connection-face manner to a plurality of connection-to-substrate terminals of the IC-chip-carrying printed wiring substrate.

4. (Twice Amended) A printed wiring substrate having a planar surface and a built-in capacitor distinct from the printed wiring substrate for mounting an IC chip or IC-chip-carrying

printed wiring substrate having a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals, said printed wiring substrate comprising a capacitor accommodation cavity for accommodating the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals projecting beyond the planar surface of the printed wiring substrate capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner to a plurality of connection-to-capacitor terminals of the IC chip or IC-chip-carrying printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups; and

the printed wiring substrate comprises a plurality of substrate terminals capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner directly to a plurality of connection-to-substrate terminals of the IC chip or IC-chip-carrying printed wiring substrate.